Extending Lasers to Universal Gates for Photonic FPGAs

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The photonic field programmable gate array (P-FPGA) is an all-optical integrated circuit that has the reprogrammability of software and the algorithm acceleration of application-specific hardware. The P-FPGA is a core enabling technology because of its speed and versatility (Fig. 1). Compared to electronic FPGAs, computational and functional reprogramming speeds are one to two and three to four orders of magnitude faster, respectively, and so we expect a proportional speedup in signal processing, encryption, graphics rendering, or genetic algorithms. Other advantages are efficient gate usage, EMI insensitivity, and direct compatibility with optical signals used in communications and photonic sensors.

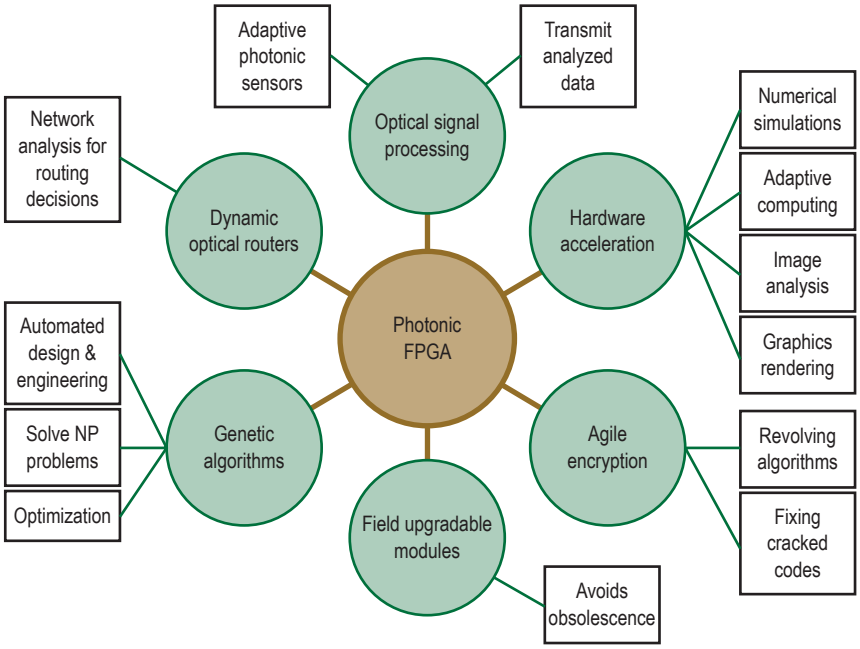

Figure 1. The P-FPGA, a core enabling technology that will enhance system performance.

The basic array element of the P-FPGA is the reconfigurable universal logic gate (Fig. 2). With feedback, the gate can act as an optical clock source or as a SET-RESET flip-flop, *i.e.*, a single bit of memory. The gate is a multiple section quantum well laser, with three lateral input optical ports with a gate selection, and two lasing outputs. The specific logic operation performed by the gate is optically selectable. The mirrors are sampled grating distributed Bragg reflectors (SG-DBRs) configured to let the output facet alternate as the laser wavelength is tuned by the optical inputs. The mirrors and phase control sections are blue-shifted by quantum well intermixing (QWI) and thus are non-absorbing at the laser wavelength. The control and slave sections provide optical gain for the circulating power.

In summary, the critical effects in the device operation are: 1) special AR/HR mirrors to create an alternating output facet laser; 2) vernier effect to reduce tuning power, so that small refractive index change causes alignment of phase with round-trip gain to jump to the next wavelength; and 3) gain-index lever to reduce tuning power and generate enhanced wavelength modulation efficiency in multiple section lasers.

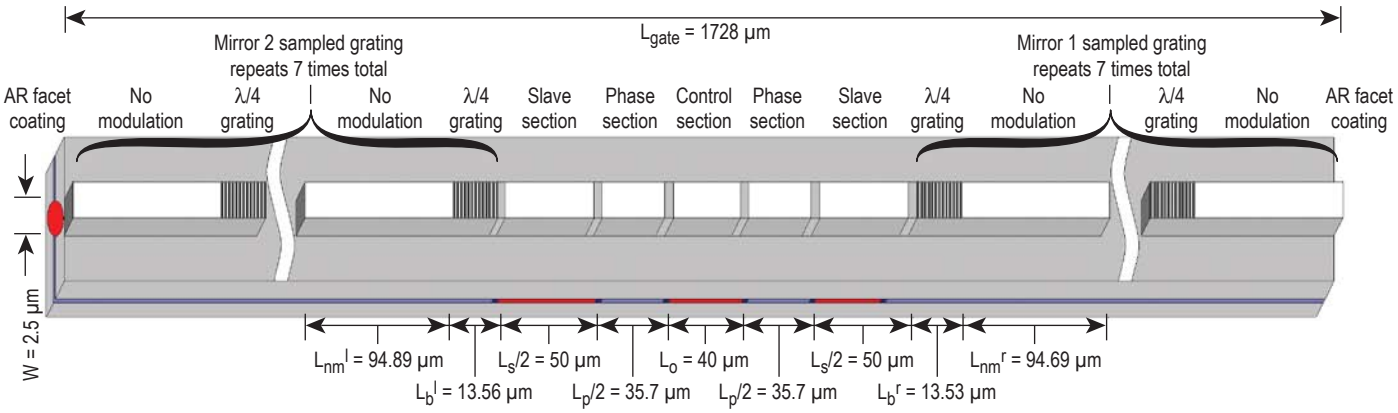

Figure 2. Layout (not to scale) for a universal logic gate. Laser output is the red ellipse. The active layer is shown in red. The active layers for the mirrors and the phase control section have been slightly blue-shifted using quantum well intermixing and are shown in medium blue. Heavily intermixed section boundaries are shown in dark blue.

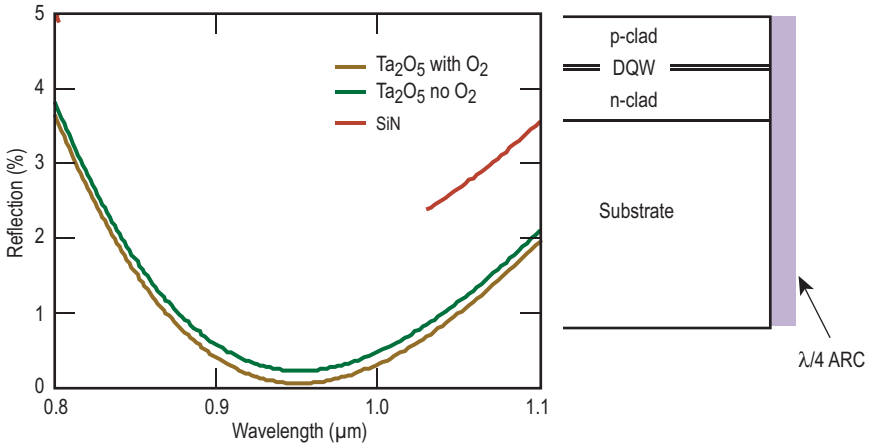

Figure 3. AR coating ellipsometry measurement results. The value n = 1.904 for Ta_2O_5 with the O_5 backfill is the best (R_{min}<0.1% and R<1% over 150 nm allows slight inaccuracies in λ/4 film thickness).

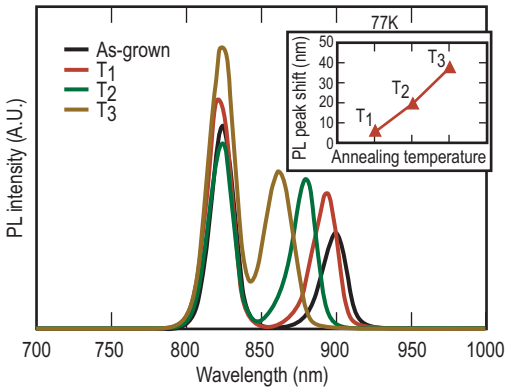

Figure 4. Photoluminescence (PL) of QWI for different annealing temperatures. PL excitation is 532 nm DPSS laser with excitation density 200 W/cm^2. Visible are the first peak (left) from GaAs and the second peak from InGaAs DQW. PL peak intensities increase after intermixing; a 38-nm shift is achieved at T_3 (inset).

Project Goals

This project focuses on establishing and troubleshooting some of the fundamental processing steps in a fairly complex fabrication procedure in order to reduce the universal gate to practice. Several of these processing steps (*e.g.*, etched facet lasers, low-loss passive waveguides, mode-matched laser to waveguide interfaces, and waveguide turning mirrors) are routinely performed on site. The four other necessary capabilities are: deposition of AR λ/4 coatings on etched facet lasers; mounting samples on patterned heat sinks; performing QWI; and defining SG-DBRs. The acquired techniques and professional relationships will expand LLNL's processing capabilities and will be valuable to future projects.

Relevance to LLNL Mission

The two applications of the P-FPGA of most interest to LLNL are implementing hardware-accelerated algorithms and processing data from photonics-based sensors because of their benefit to many Laboratory core applications. Some sample hardware-accelerated algorithms are 1) self-evolving genetic algorithms for efficiently solving NP problems; 2) adaptive computing for enhanced speed in computationally intensive simulations or graphics rendering; and 3) reconfigurable encryption algorithms for secure communications, *e.g.*, constantly changing encryption algorithms or repairing broken algorithms in field deployed units. On-chip data processing would expand the capabilities of all photonics-based sensors created at the Laboratory. For example, the sensors can adapt or make decisions based on collected data, or could transmit analyzed data rather than raw images when the downlink bandwidth is limited.

FY2007 Accomplishments and Results

We have accomplished the following: 1) completed AR coating and gratings configurations; 2) characterized AR coatings and demonstrated a vertical facet deposition procedure (Fig. 3); 3) purchased, patterned, and evaluated heat sinks; 4) specified and procured a five-mask set; 5) established a collaboration to perform QWI and observe induced blue shift (Fig. 4); 6) fabricated multi-section lasers with new engineered epitaxial material and a new chemical etch recipe to handle an InGaP stop layer (Fig. 5); and 7) implemented and used automatic measurement and post-processing techniques to evaluate the gain-index lever effect.

Related References

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4. Goddard, L., *et al.*, "Rapidly Reconfigurable All-Optical Universal Logic Gates," *Proc. SPIE*, **6368**, pp. 6368 OH-1-13, October 2006.

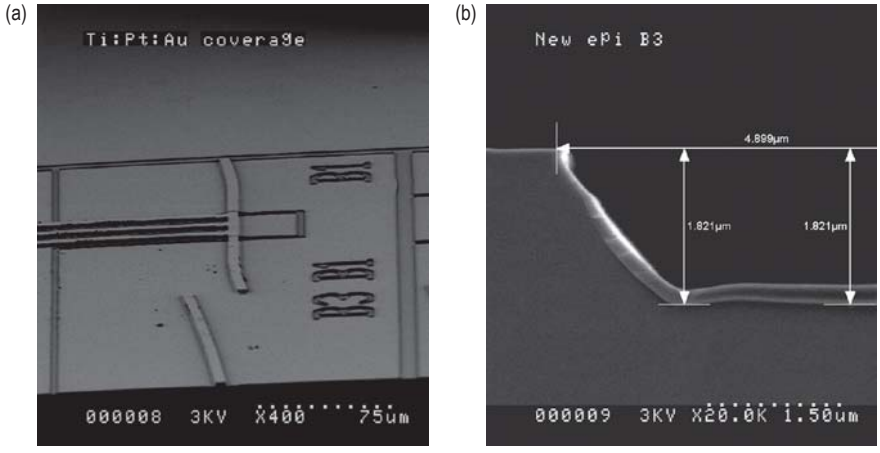

Figure 5. SEM of (a) 3-side input InGaAs QW laser; and (b) lateral ridge etch.